

**High-Speed CMOS Logic  
4-Bit Bidirectional Universal Shift Register**

**Features**

- **Four Operating Modes**
  - Shift Right, Shift Left, Hold and Reset
- **Synchronous Parallel or Serial Operation**
- **Typical  $f_{MAX} = 60\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$**
- **Asynchronous Master Reset**
- **Fanout (Over Temperature Range)**
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- **Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- **HCT Types**
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V}$  (Max),  $V_{IH} = 2\text{V}$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

**Description**

The 'HC194 and CD74HCT194 are 4-bit shift registers with Asynchronous Master Reset ( $\overline{\text{MR}}$ ). In the parallel mode ( $S_0$  and  $S_1$  are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP). During parallel loading serial data flow is inhibited. Shift left and shift right are accomplished synchronously on the positive clock edge with serial data entered at the shift left (DSL) serial input for the shift right mode, and at the shift right (DSR) serial input for the shift left mode. Clearing the register is accomplished by a Low applied to the Master Reset ( $\overline{\text{MR}}$ ) pin.

**Ordering Information**

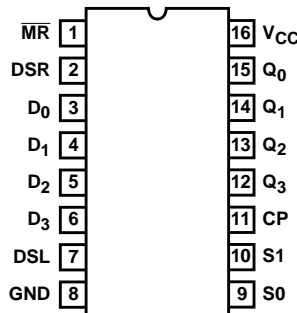
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC194F3A	-55 to 125	16 Ld CERDIP
CD74HC194E	-55 to 125	16 Ld PDIP
CD74HC194M	-55 to 125	16 Ld SOIC
CD74HC194NSR	-55 to 125	16 Ld SOP
CD74HCT194E	-55 to 125	16 Ld PDIP

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

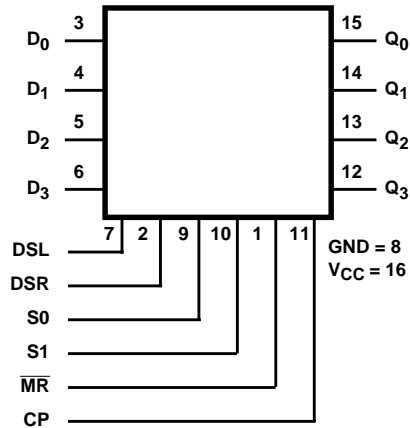
**Pinout**

CD54HC194  
(CERDIP)  
CD74HC194  
(PDIP, SOIC, SOP)  
CD74HCT194  
(PDIP, SOIC)  
TOP VIEW



## CD54/74HC194, CD74HCT194

### Functional Diagram



TRUTH TABLE

OPERATING MODE	INPUTS							OUTPUT			
	CP	$\overline{\text{MR}}$	S1	S0	DSR	DSL	$D_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
Reset (Clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (Do Nothing)	X	H	I (Note 2)	I (Note 2)	X	X	X	$q_0$	$q_1$	$q_2$	$q_3$
Shift Left	$\uparrow$	H	h	I (Note 2)	X	l	X	$q_1$	$q_2$	$q_3$	L
	$\uparrow$	H	h	I (Note 2)	X	h	X	$q_1$	$q_2$	$q_3$	H
Shift Right	$\uparrow$	H	I (Note 2)	h	l	X	X	L	$q_0$	$q_1$	$q_2$
	$\uparrow$	H	I (Note 2)	h	h	X	X	H	$q_0$	$q_1$	$q_2$
Parallel Load	$\uparrow$	H	h	h	X	X	$d_n$	$d_0$	$d_1$	$q_2$	$d_3$

**NOTES:**

1. H = High Voltage Level,  
 h = High Voltage Level One Set-up Time Prior To The Low to High Clock Transition,  
 L = Low Voltage Level,  
 l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition,  
 $d_n$  ( $q_n$ ) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low To High Clock Transition,  
 X = Don't Care,  
 $\uparrow$  = Transition from Low to High Level
2. The High to Low transition of the S0 and S1 Inputs on the 'HC194, CD74HCT194 should only take place while CP is High for Conventional Operation.

# CD54/74HC194, CD74HCT194

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

## Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 3):	
PDIP Package .....	67°C/W
SOIC Package .....	73°C/W
SOP Package .....	64°C/W
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C
(SOIC - Lead Tips Only)	

## Operating Conditions

Temperature Range ( $T_A$ ) .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

## CD54/74HC194, CD74HCT194

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

4. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
CP	0.6
MR	0.55
DSL, DSR, D <sub>n</sub>	0.25
Sn	1.10

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

## CD54/74HC194, CD74HCT194

### Prerequisite For Switching Function

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
Max. Clock Frequency (Figure 1)	f <sub>MAX</sub>	-	2	6	-	5	-	4	-	MHz
			4.5	30	-	24	-	20	-	MHz
			6	35	-	28	-	23	-	MHz
MR Pulse Width (Figure 2)	t <sub>W</sub>	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Clock Pulse Width (Figure 1)	t <sub>W</sub>	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Set-up Time Data to Clock (Figure 3)	t <sub>SU</sub>	-	2	70	-	90	-	105	-	ns
			4.5	14	-	18	-	21	-	ns
			6	12	-	15	-	19	-	ns
Removal Time, MR to Clock (Figure 2)	t <sub>REM</sub>	-	2	60	-	75	-	90	-	ns
			4.5	12	-	15	-	18	-	ns
			6	10	-	13	-	15	-	ns
Set-Up Time S1, S0 to Clock (Figure 4)	t <sub>SU</sub>	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Set-up Time DSL, DSR to Clock (Figure 4)	t <sub>SU</sub>	-	2	70	-	90	-	105	-	ns
			4.5	14	-	18	-	21	-	ns
			6	12	-	15	-	18	-	ns
Hold Time S1, S0 to Clock (Figure 4)	t <sub>H</sub>	-	2	0	-	0	-	0	-	ns
			4.5	0	-	0	-	0	-	ns
			6	0	-	0	-	0	-	ns
Hold Time Data to Clock (Figure 3)	t <sub>H</sub>	-	2	0	-	0	-	0	-	ns
			4.5	0	-	0	-	0	-	ns
			6	0	-	0	-	0	-	ns
<b>HCT TYPES</b>										
Max. Clock Frequency (Figure 1)	f <sub>MAX</sub>	-	4.5	27	-	22	-	18	-	MHz
MR Pulse Width (Figure 2)	t <sub>W</sub>	-	4.5	16	-	20	-	24	-	ns
Clock Pulse Width (Figure 1)	t <sub>W</sub>	-	4.5	16	-	20	-	24	-	ns
Set-up Time, Data to Clock (Figure 3)	t <sub>SU</sub>	-	4.5	14	-	18	-	21	-	ns
Removal Time MR to Clock (Figure 2)	t <sub>REM</sub>	-	4.5	12	-	15	-	18	-	ns

## CD54/74HC194, CD74HCT194

### Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
Set-up Time S1, S0 to Clock (Figure 4)	t <sub>SU</sub>	-	4.5	20	-	25	-	30	-	ns
Set-up Time DSL, DSR to Clock (Figure 4)	t <sub>SU</sub>	-	4.5	14	-	18	-	21	-	ns
Hold Time S1, S0 to Clock (Figure 4)	t <sub>H</sub>	-	4.5	0	-	0	-	0	-	ns
Hold Time Data to Clock (Figure 3)	t <sub>H</sub>	-	4.5	0	-	0	-	0	-	ns

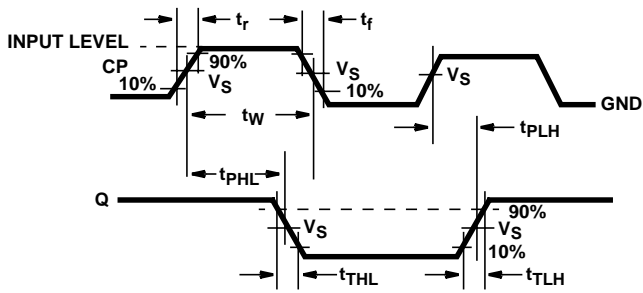
### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay, Clock to Output (Figure 1)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	37	45	ns
Propagation Delay, Clock to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	-	5	14	-	-	-	ns
Output Transition Time (Figure 1)	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Propagation Delay, MR to Output (Figure 2)	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	140	175	210	ns
			4.5	-	28	35	42	ns
			6	-	24	30	36	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	10	10	10	pF
Maximum Clock Frequency	f <sub>MAX</sub>	-	5	60	-	-	-	MHz
Power Dissipation Capacitance (Notes 5, 6)	C <sub>PD</sub>	-	5	55	-	-	-	pF
<b>HCT TYPES</b>								
Propagation Delay, Clock to Output (Figure 1)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	37	46	56	ns
Propagation Delay, Clock to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	-	5	15	-	-	-	ns
Output Transition Times (Figure 1)	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	4.5	-	15	19	22	ns
Propagation Delay, MR to Output (Figure 2)	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	40	50	60	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	10	10	10	pF
Maximum Clock Frequency	f <sub>MAX</sub>	-	5	50	-	-	-	MHz
Power Dissipation Capacitance (Notes 5, 6)	C <sub>PD</sub>	-	5	60	-	-	-	pF

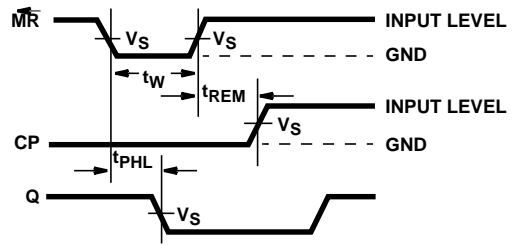
**NOTES:**

5. C<sub>PD</sub> is used to determine the dynamic power consumption, per gate.
6.  $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2)$  where f<sub>i</sub> = Input Frequency, C<sub>L</sub> = Output Load Capacitance, V<sub>CC</sub> = Supply Voltage.

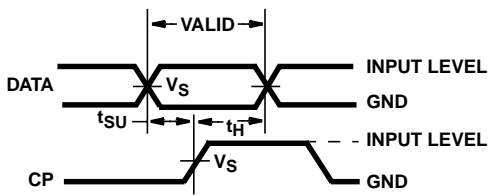
**Test Circuits and Waveforms**



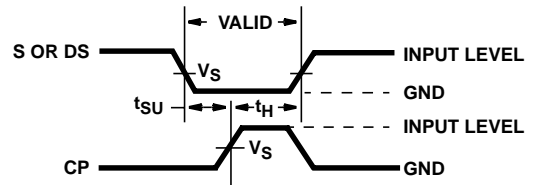
**FIGURE 1. CLOCK PRE-REQUISITE TIMES AND PROPAGATION AND OUTPUT TRANSITION TIMES**



**FIGURE 2. MASTER RESET PRE-REQUISITE TIMES AND PROPAGATION DELAYS**



**FIGURE 3. DATA PRE-REQUISITE TIMES**



**FIGURE 4. PARALLEL LOAD OR SHIFT-LEFT/SHIFT-RIGHT PRE-REQUISITE TIMES**