

# SN74LS161A SN74LS163A

## BCD Decade Counters/ 4-Bit Binary Counters

The LS161A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS161A and LS163A count modulo 16 (binary).

The LS161A has an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS163A has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	Binary (Modulo 16)
Asynchronous Reset	LS161A
Synchronous Reset	LS163A

- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Edge-Triggered Operation
- Typical Count Rate of 35 MHz
- ESD > 3500 Volts

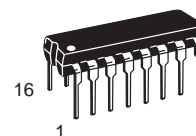
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

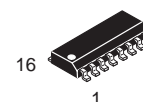


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Formerly a Division of Motorola  
<http://onsemi.com>

### LOW POWER SCHOTTKY



**PLASTIC  
N SUFFIX  
CASE 648**



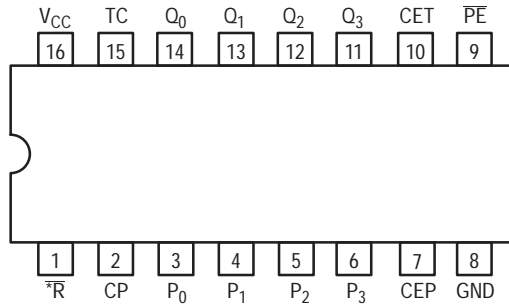
**SOIC  
D SUFFIX  
CASE 751B**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS161AN	16 Pin DIP	2000 Units/Box
SN74LS161AD	16 Pin	2500/Tape & Reel
SN74LS163AN	16 Pin DIP	2000 Units/Box
SN74LS163AD	16 Pin	2500/Tape & Reel

# SN74LS161A SN74LS163A

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

\*MR for LS161A  
\*SR for LS163A

### PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
$P_0 - P_3$	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$\overline{SR}$	Synchronous Reset (Active LOW) Input
$Q_0 - Q_3$	Parallel Outputs
TC	Terminal Count Output

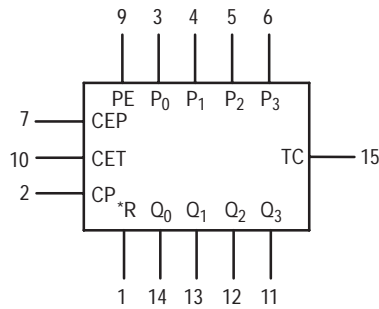
### LOADING (Note a)

	HIGH	LOW
$\overline{PE}$	1.0 U.L.	0.5 U.L.
$P_0 - P_3$	0.5 U.L.	0.25 U.L.
CEP	0.5 U.L.	0.25 U.L.
CET	1.0 U.L.	0.5 U.L.
CP	0.5 U.L.	0.25 U.L.
$\overline{MR}$	0.5 U.L.	0.25 U.L.
$\overline{SR}$	1.0 U.L.	0.5 U.L.
$Q_0 - Q_3$	10 U.L.	5 U.L.
TC	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL

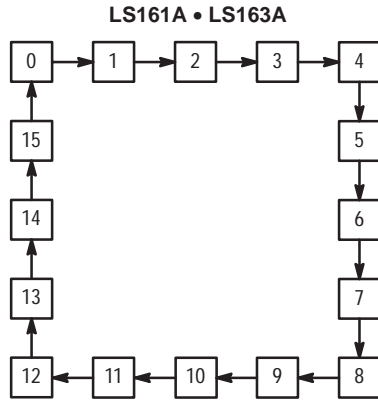


$V_{CC}$  = PIN 16  
GND = PIN 8

\*MR for LS161A  
\*SR for LS163A

# SN74LS161A SN74LS163A

## STATE DIAGRAM



### LOGIC EQUATIONS

Count Enable =  $CEP \cdot CET \cdot PE$

TC for LS161A & LS163A =  $CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$

Preset =  $\overline{PE} \cdot CP +$  (rising clock edge)

Reset =  $\overline{MR}$  (LS161A)

Reset =  $\overline{SR} \cdot CP +$  (rising clock edge)  
(LS163A)

## FUNCTIONAL DESCRIPTION

The LS161A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. The counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable ( $\overline{PE}$ ), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and  $\overline{PE}$  inputs are HIGH. When the  $\overline{PE}$  is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the  $\overline{PE}$  held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs ( $CET \cdot CEP$ ) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ( $\overline{MR}$ ) of the LS161A is asynchronous. When the  $\overline{MR}$  is LOW, it overrides all other input conditions and sets the outputs LOW. The  $\overline{MR}$  pin should never be left open. If not used, the  $\overline{MR}$  pin should be tied through a resistor to  $V_{CC}$ , or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ( $\overline{SR}$ ) input of the LS163A acts as an edge-triggered control input, overriding CET, CEP and  $\overline{PE}$ , and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge ( $\uparrow$ )
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ( $P_n$ $Q_n$ )
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

\*For the LS163A only.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

# SN74LS161A SN74LS163A

## LS161A

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current MR, Data, CEP, Clock PE, CET			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	MR, Data, CEP, Clock PE, CET			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current MR, Data, CEP, Clock PE, CET			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## LS163A

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current Data, CEP, Clock PE, CET, SR			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	Data, CEP, Clock PE, CET, SR			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current Data, CEP, Clock, PE, SR CET			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS161A SN74LS163A

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	25	32		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to TC		20 18	35 35	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Q		13 18	24 27	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t <sub>PHL</sub>	$\overline{MR}$ or $\overline{SR}$ to Q		20	28	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>WCP</sub>	Clock Pulse Width Low	25			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	$\overline{MR}$ or $\overline{SR}$ Pulse Width	20			ns	
t <sub>s</sub>	Setup Time, other*	20			ns	
t <sub>s</sub>	Setup Time PE or SR	25			ns	
t <sub>h</sub>	Hold Time, data	3			ns	
t <sub>h</sub>	Hold Time, other	0			ns	
t <sub>rec</sub>	Recovery Time $\overline{MR}$ to CP	15			ns	

\*CEP, CET, or DATA

## DEFINITION OF TERMS

**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

**RECOVERY TIME (t<sub>rec</sub>)** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

## AC WAVEFORMS

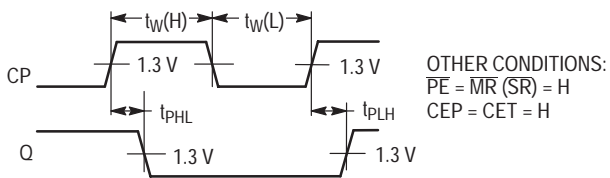


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

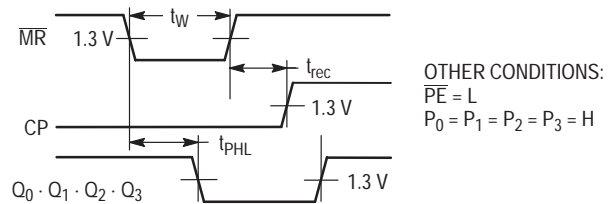


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

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## AC WAVEFORMS (continued)

### COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the ( $Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$ ) state for the LS161 and LS163.

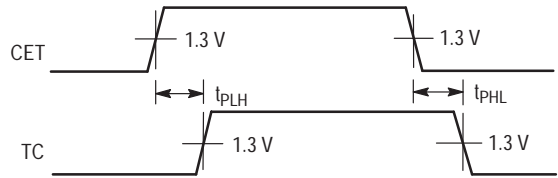


Figure 3.

OTHER CONDITIONS:  $CP = \overline{PE} = CEP = \overline{MR} = H$

### CLOCK TO TERMINAL COUNT DELAYS

The positive TC pulse is coincident with the output state ( $Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$ ) for the LS161 and LS163.

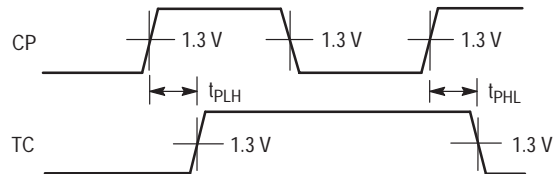


Figure 4.

OTHER CONDITIONS:  $\overline{PE} = CEP = CET = \overline{MR} = H$

### SETUP TIME ( $t_s$ ) AND HOLD TIME ( $t_h$ ) FOR PARALLEL DATA INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

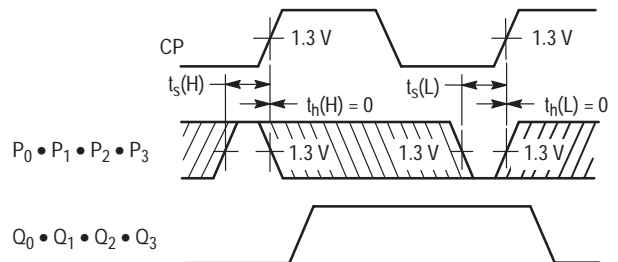


Figure 5.

OTHER CONDITIONS:  $\overline{PE} = L, \overline{MR} = H$

### SETUP TIME ( $t_s$ ) AND HOLD TIME ( $t_h$ ) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ( $\overline{PE}$ ) INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

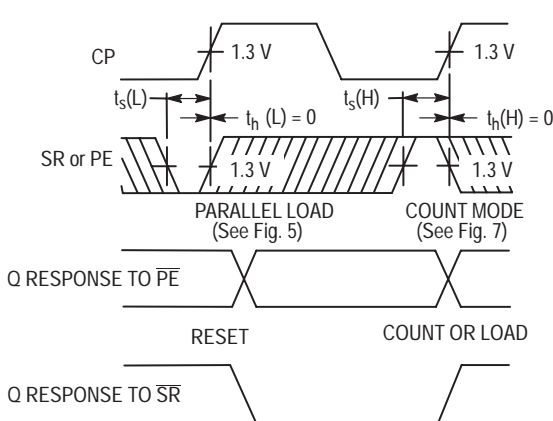


Figure 6.

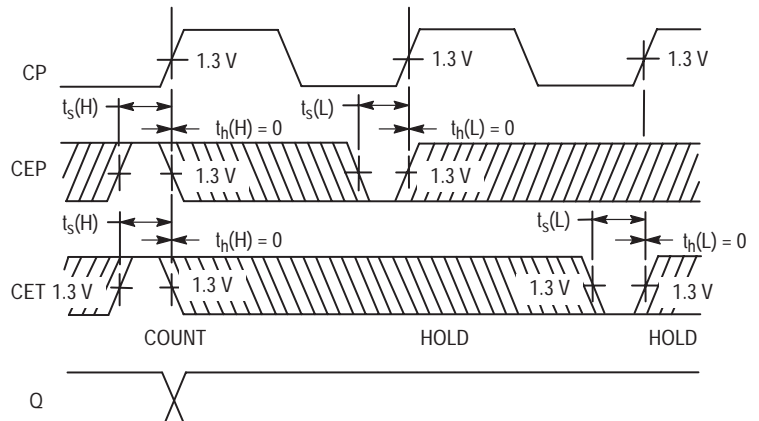


Figure 7.

OTHER CONDITIONS:  $\overline{PE} = H, \overline{MR} = H$