

# SN74LS257B SN74LS258B

## Quad 2-Input Multiplexer with 3-State Outputs

The LSTTL/MSI SN74LS257B and the SN74LS258B are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ( $E_O$ ) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process For High Speed
- Multiplexer Expansion By Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

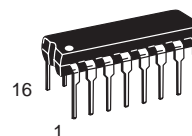
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current – High			-2.6	mA
$I_{OL}$	Output Current – Low			24	mA

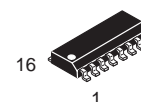


**ON Semiconductor**  
Formerly a Division of Motorola  
<http://onsemi.com>

**LOW  
POWER  
SCHOTTKY**



PLASTIC  
N SUFFIX  
CASE 648



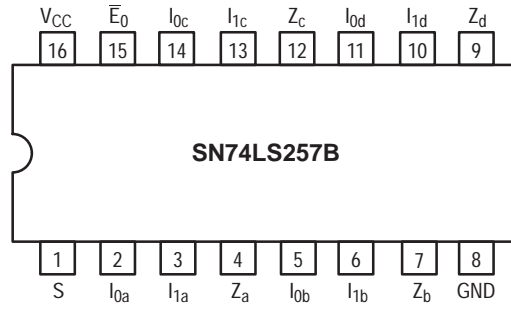
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

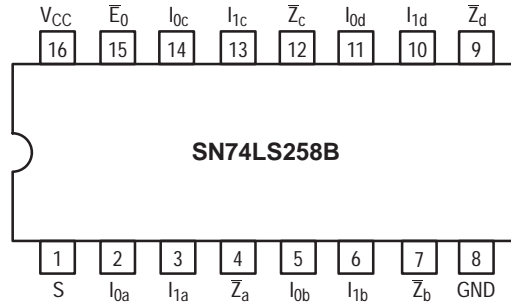
Device	Package	Shipping
SN74LS257BN	16 Pin DIP	2000 Units/Box
SN74LS257BD	16 Pin	2500/Tape & Reel
SN74LS258BN	16 Pin DIP	2000 Units/Box
SN74LS258BD	16 Pin	2500/Tape & Reel

# SN74LS257B SN74LS258B

## CONNECTION DIAGRAM DIP (TOP VIEW)



V<sub>CC</sub> = PIN 16  
GND = PIN 8

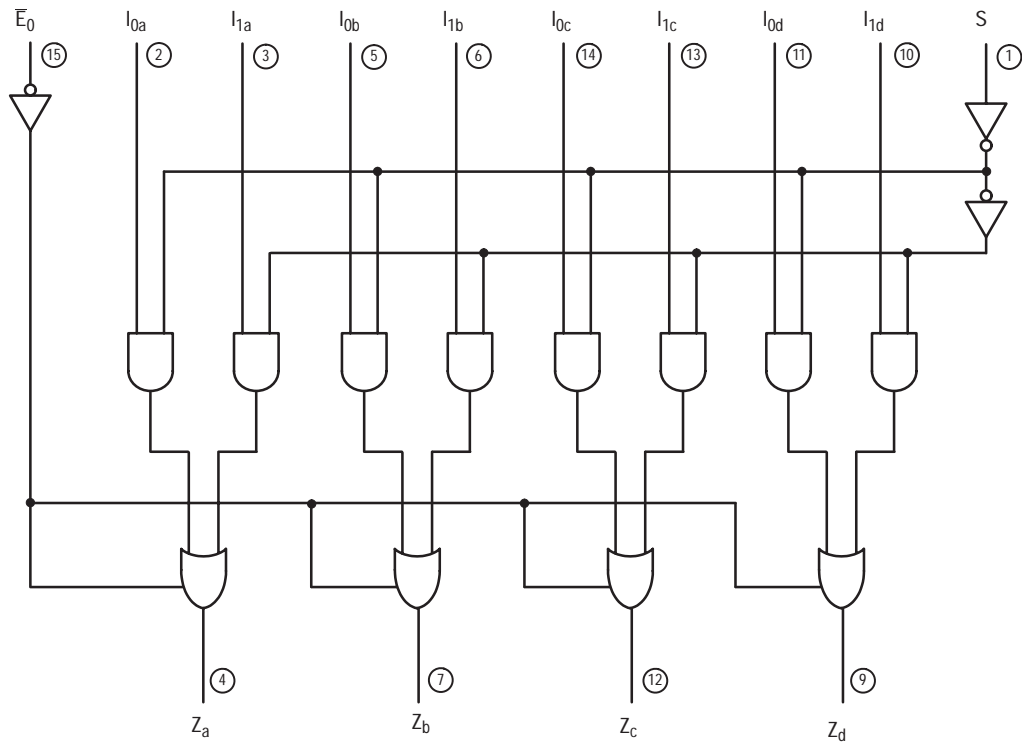


NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

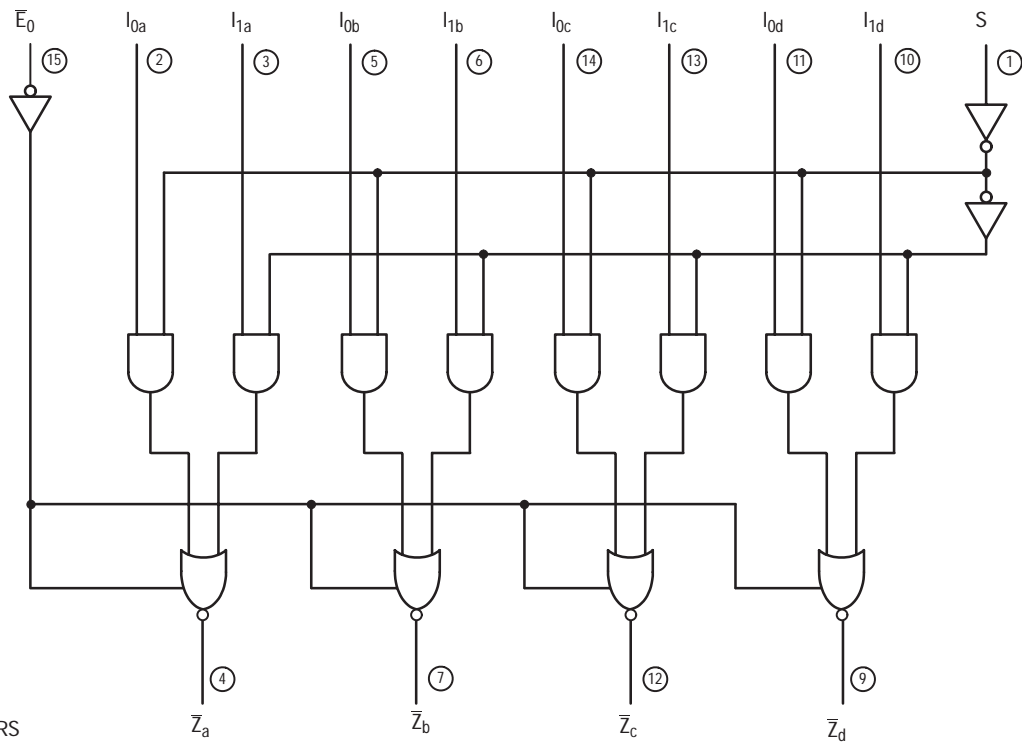
# SN74LS257B SN74LS258B

## LOGIC DIAGRAMS

### SN74LS257B



### SN74LS258B



$V_{CC}$  = PIN 16  
GND = PIN 8  
○ = PIN NUMBERS

## SN74LS257B SN74LS258B

### FUNCTIONAL DESCRIPTION

The LS257B and LS258B are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the I<sub>0</sub> inputs are selected and when Select is HIGH, the I<sub>1</sub> inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257B and in the inverted form for the LS258B.

The LS257B and LS258B are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

#### LS257B

$$\begin{aligned} Z_a &= \bar{E}_0 \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ Z_b &= \bar{E}_0 \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ Z_c &= \bar{E}_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ Z_d &= \bar{E}_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

When the Output Enable Input ( $\bar{E}_0$ ) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

#### LS258B

$$\begin{aligned} \bar{Z}_a &= \bar{E}_0 \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ \bar{Z}_b &= \bar{E}_0 \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ \bar{Z}_c &= \bar{E}_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ \bar{Z}_d &= \bar{E}_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS LS257B	OUTPUTS LS258B
$\bar{E}_0$	S	I <sub>0</sub>	I <sub>1</sub>	Z	$\bar{Z}$
H	X	X	X	(Z)	(Z)
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 (Z) = High Impedance (off)

# SN74LS257B SN74LS258B

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4	3.1		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 12 mA
			0.35	0.5	V	I <sub>OL</sub> = 24 mA
I <sub>OZH</sub>	Output Off Current — HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V
I <sub>OZL</sub>	Output Off Current — LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current Other Inputs S Inputs			20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	Other Inputs S Inputs			0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current All Inputs			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-30		-130	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH	LS257B LS258B		10 9.0	mA	V <sub>CC</sub> = MAX
	Total, Output LOW	LS257B LS258B		16 14	mA	
	Total, Output 3-State	LS257B LS258B		19 16	mA	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V) See SN74LS251 for Waveforms

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output		10 12	13 15	ns	Figures 1 & 2	C <sub>L</sub> = 45 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Select to Output		14 14	21 21	ns	Figures 1 & 2	
t <sub>PZH</sub>	Output Enable Time to HIGH Level		20	25	ns	Figures 4 & 5	C <sub>L</sub> = 45 pF R <sub>L</sub> = 667 Ω
t <sub>PZL</sub>	Output Enable Time to LOW Level		20	25	ns	Figures 3 & 5	
t <sub>PLZ</sub>	Output Disable Time to LOW Level		16	25	ns	Figures 3 & 5	C <sub>L</sub> = 5.0 pF R <sub>L</sub> = 667 Ω
t <sub>PHZ</sub>	Output Disable Time from HIGH Level		18	25	ns	Figures 4 & 5	