

SN74LS259

8-Bit Addressable Latch

The SN74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

- Serial-to-Parallel Conversion
- Eight Bits of Storage With Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

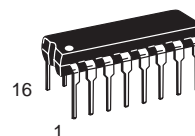
GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			-0.4	mA
I_{OL}	Output Current – Low			8.0	mA

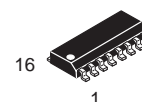


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**LOW
POWER
SCHOTTKY**



**PLASTIC
N SUFFIX
CASE 648**



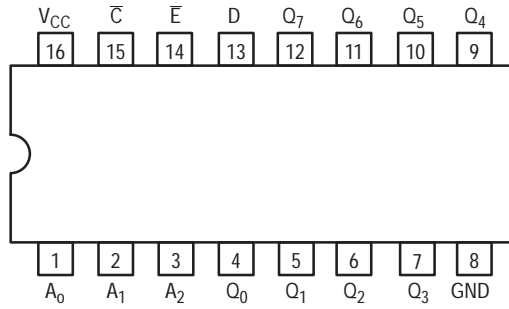
**SOIC
D SUFFIX
CASE 751B**

ORDERING INFORMATION

Device	Package	Shipping
SN74LS259N	16 Pin DIP	2000 Units/Box
SN74LS259D	16 Pin	2500/Tape & Reel

SN74LS259

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

A_0, A_1, A_2	Address Inputs
D	Data Input
\bar{E}	Enable (Active LOW) Input
\bar{C}	Clear (Active LOW) Input
$Q_0 - Q_7$	Parallel Latch Outputs

LOADING (Note a)

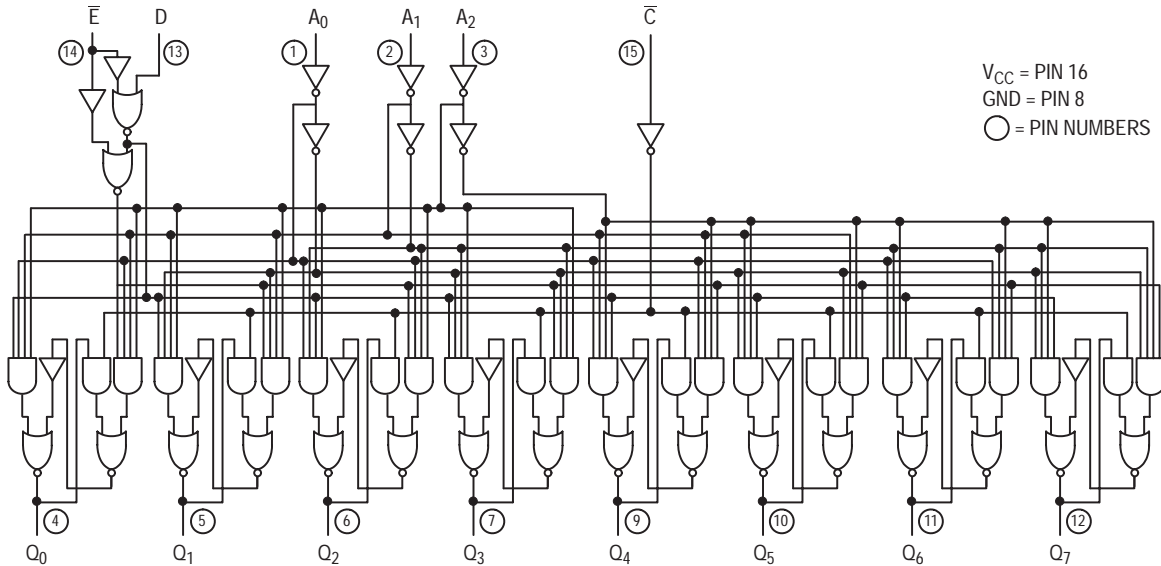
	HIGH	LOW
A_0, A_1, A_2	0.5 U.L.	0.25 U.L.
D	0.5 U.L.	0.25 U.L.
\bar{E}	1.0 U.L.	0.5 U.L.
\bar{C}	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	10 U.L.	5 U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

SN74LS259

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all

other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the SN74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations.

MODE SELECTION

E	C̄	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

PRESENT OUTPUT STATES

C̄	E	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	MODE	
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear Demultiplex	
L	L	H	L	L	L	H	L	L	L	L	L	L	L		
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Memory	
L	L	H	H	L	L	L	H	L	L	L	L	L	L		
L	L	H	H	H	H	L	L	L	L	L	L	L	H	Memory	
H	H	X	X	X	X	Q _{N-1}	→								Memory
H	L	L	L	L	L	L	Q _{N-1}	Q _{N-1}	Q _{N-1}	Q _{N-1}	→			Addressable Latch	
H	L	H	L	L	L	H	Q _{N-1}	Q _{N-1}	Q _{N-1}	→					
H	L	L	H	L	L	Q _{N-1}	L	Q _{N-1}	Q _{N-1}	→					
H	L	H	H	L	L	Q _{N-1}	H	Q _{N-1}	Q _{N-1}	→					
•	•	•	•	•	•	•	•	•	•	•	•	•	•	Addressable Latch	
•	•	•	•	•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•	•	•	•	•		
H	L	L	H	H	H	Q _{N-1}	→						Q _{N-1}	L	Addressable Latch
H	L	H	H	H	H	Q _{N-1}	→						Q _{N-1}	H	

X = Don't Care Condition
 L = LOW Voltage Level
 H = HIGH Voltage Level
 Q_{N-1} = Previous Output State

SN74LS259

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.7	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
			0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current			36	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

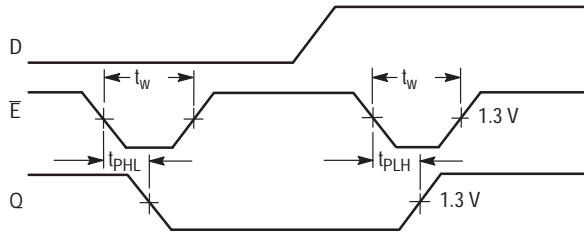
AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Turn-Off Delay, Enable to Output Turn-On Delay, Enable to Output		22 15	35 24	ns ns	C _L = 15 pF
t _{PLH} t _{PHL}	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	32 21	ns ns	
t _{PLH} t _{PHL}	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		24 18	38 29	ns ns	
t _{PHL}	Turn-On Delay, Clear to Output		17	27	ns	

AC SET-UP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

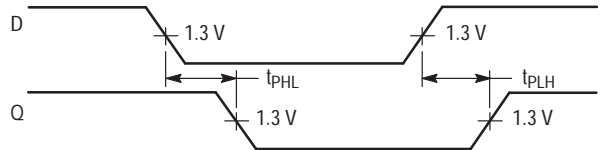
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t _s	Input Setup Time	20			ns
t _w	Pulse Width, Clear or Enable	15			ns
t _h	Hold Time, Data	5.0			ns
t _h	Hold Time, Address	20			ns

AC WAVEFORMS



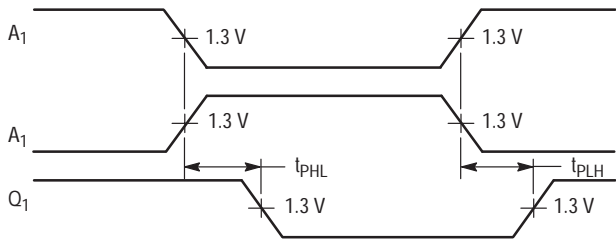
OTHER CONDITIONS: $\bar{C} = H, A = \text{STABLE}$

Figure 1. Turn-on and Turn-off Delays, Enable To Output and Enable Pulse Width



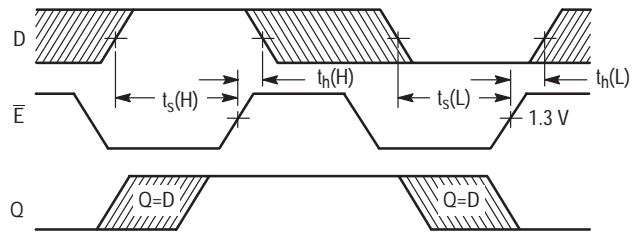
OTHER CONDITIONS: $\bar{E} = L, \bar{C} = H, A = \text{STABLE}$

Figure 2. Turn-on and Turn-off Delays, Data to Output



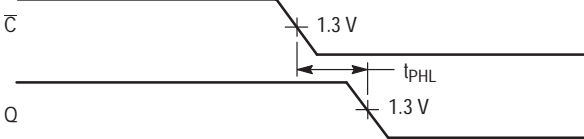
OTHER CONDITIONS: $\bar{E} = L, \bar{C} = L, D = H$

Figure 3. Turn-on and Turn-off Delays, Address to Output



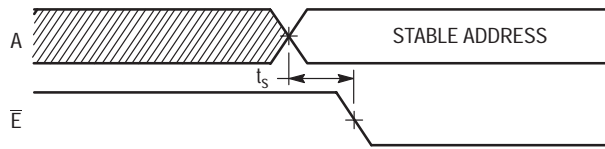
OTHER CONDITIONS: $\bar{C} = H, A = \text{STABLE}$

Figure 4. Setup and Hold Time, Data to Enable



OTHER CONDITIONS: $\bar{E} = H$

Figure 5. Turn-on Delay, Clear to Output



OTHER CONDITIONS: $\bar{C} = H$

Figure 6. Setup Time, Address to Enable (See Notes 1 and 2)

NOTES:

1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.