

SN74LS299

8-Bit Shift/Storage Register with 3-State Outputs

The SN74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High Q_0, Q_7			-0.4	mA
I_{OL}	Output Current – Low Q_0, Q_7			8.0	mA
I_{OH}	Output Current – High $I/O_0 - I/O_7$			-2.6	mA
I_{OL}	Output Current – Low $I/O_0 - I/O_7$			24	mA

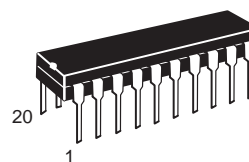


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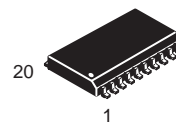
Formerly a Division of Motorola

<http://onsemi.com>

**LOW
POWER
SCHOTTKY**



**PLASTIC
N SUFFIX
CASE 738**



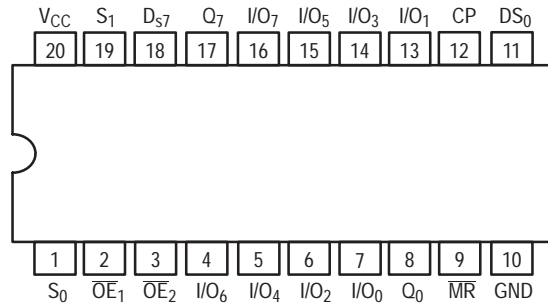
**SOIC
DW SUFFIX
CASE 751D**

ORDERING INFORMATION

Device	Package	Shipping
SN74LS299N	16 Pin DIP	1440 Units/Box
SN74LS299DW	16 Pin	2500/Tape & Reel

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CONNECTION DIAGRAM DIP (TOP VIEW)

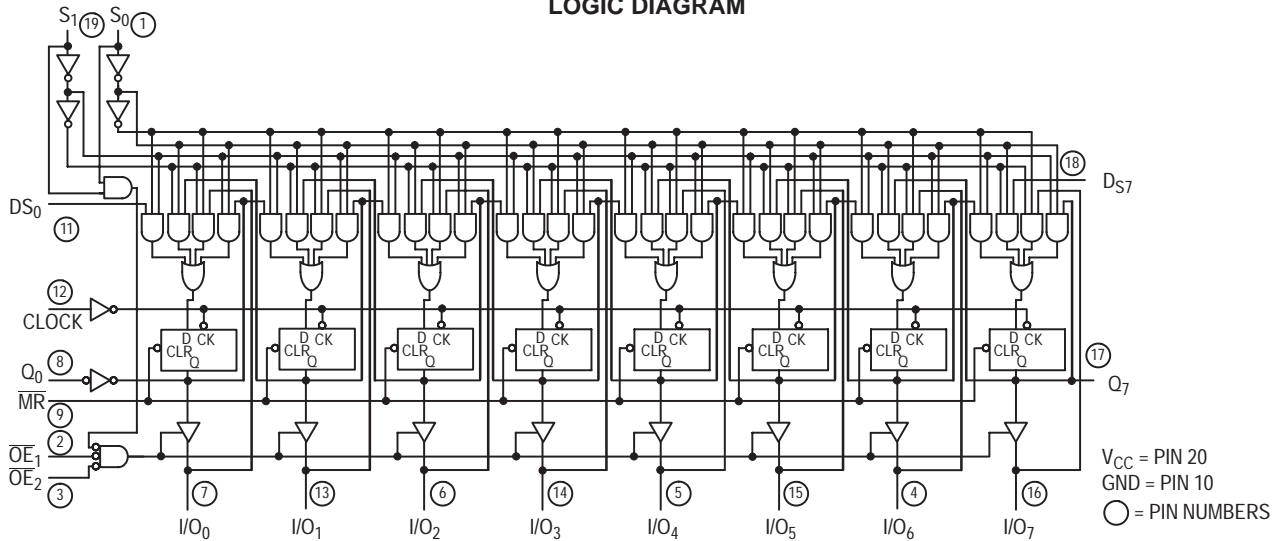


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
CP	Clock Pulse (Active Positive-Going Edge) Input	0.5 U.L.	0.25 U.L.
DS0	Serial Data Input for Right Shift	0.5 U.L.	0.25 U.L.
DS7	Serial Data Input for Left Shift	0.5 U.L.	0.25 U.L.
I/O _n	Parallel Data Input or Parallel Output (3-State)	0.5 U.L.	0.25 U.L.
		65 U.L.	15 U.L.
$\overline{OE}_1, \overline{OE}_2$	3-State Output Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
Q ₀ , Q ₇	Serial Outputs	10 U.L.	5 U.L.
\overline{MR}	Asynchronous Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
S ₀ , S ₁	Mode Select Inputs	1 U.L.	0.5 U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

LOGIC DIAGRAM



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FUNCTION TABLE

INPUTS								RESPONSE
MR	S ₁	S ₀	OE ₁	OE ₂	CP	DS ₀	DS ₇	
L	X	X	H	X	X	X	X	Asynchronous Reset; Q ₀ = Q ₇ = LOW I/O Voltage Undetermined
L	X	X	X	H	X	X	X	
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Asynchronous Reset; Q ₀ = Q ₇ = LOW I/O Voltage LOW
L	X	L	L	L	X	X	X	
H	L	H	X	X	┌	D	X	Shift Right; D→Q ₀ ; Q ₀ →Q ₁ ; etc. Shift Right; D→Q ₀ & I/O ₀ ; Q ₀ →O ₁ & I/O ₁ ; etc.
H	L	H	L	L	└	D	X	
H	H	L	X	X	┌	X	D	Shift Left; D→Q ₇ ; Q ₇ →Q ₆ ; etc. Shift Left; D→Q ₇ & I/O ₇ ; Q ₇ →Q ₆ & I/O ₆ ; etc.
H	H	L	L	L	└	X	D	
H	H	H	X	X	┌	X	X	Parallel Load; I/O _n →Q _n
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: I/O _n = Q _n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage I/O ₀ -I/O ₇	2.4	3.1		V	V _{CC} = MIN, I _{OH} = MAX	
V _{OH}	Output HIGH Voltage Q ₀ , Q ₇	2.7	3.4		V	V _{CC} = MIN, I _{OH} = MAX	
V _{OL}	Output LOW Voltage I/O ₀ -I/O ₇		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
			0.35	0.5	V	I _{OL} = 24 mA	
V _{OL}	Output LOW Voltage I/O ₀ -I/O ₇			0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
				0.5	V	I _{OL} = 8.0 mA	
I _{OZH}	Output Off Current HIGH I/O ₀ -I/O ₇			40	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW I/O ₀ -I/O ₇			-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current	Others		20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		S ₀ , S ₁ , I/O ₀ -I/O ₇		40	μA		
		Others		0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
		S ₀ , S ₁		0.2	mA		
		I/O ₀ -I/O ₇		0.1	mA		
I _{IL}	Input LOW Current	Others		-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		S ₀ , S ₁		-0.8	mA		
I _{OS}	Short Circuit Current (Note 1)	Q ₀ , Q ₇	-20	-100	mA	V _{CC} = MAX	
		I/O ₀ -I/O ₇	-30	-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			53	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

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AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	35		MHz	C _L = 15 pF
t _{PHL} t _{PLH}	Propagation Delay, Clock to Q ₀ or Q ₇		26 22	39 33	ns	
t _{PHL}	Propagation Delay, Clear to Q ₀ or Q ₇		27	40	ns	
t _{PHL} t _{PLH}	Propagation Delay, Clock to I/O ₀ –I/O ₇		26 17	39 25	ns	C _L = 45 pF, R _L = 667 Ω
t _{PHL}	Propagation Delay, Clear to I/O ₀ –I/O ₇		26	40	ns	
t _{PZH} t _{PZL}	Output Enable Time		13 19	21 30	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		10 10	15 15	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width HIGH	25			ns	V _{CC} = 5.0 V
t _W	Clock Pulse Width LOW	13			ns	
t _W	Clear Pulse Width LOW	20			ns	
t _s	Data Setup Time	20			ns	
t _s	Select Setup Time	35			ns	
t _h	Data Hold Time	0			ns	
t _h	Select Hold Time	10			ns	
t _{rec}	Recovery Time	20			ns	

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3-STATE WAVEFORMS

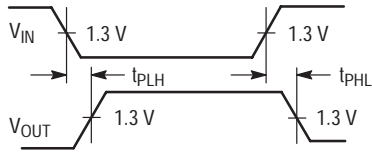


Figure 1.

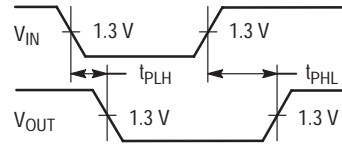


Figure 2.

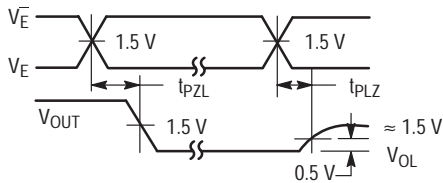


Figure 3.

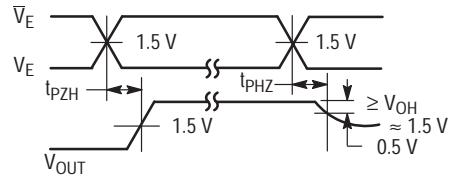
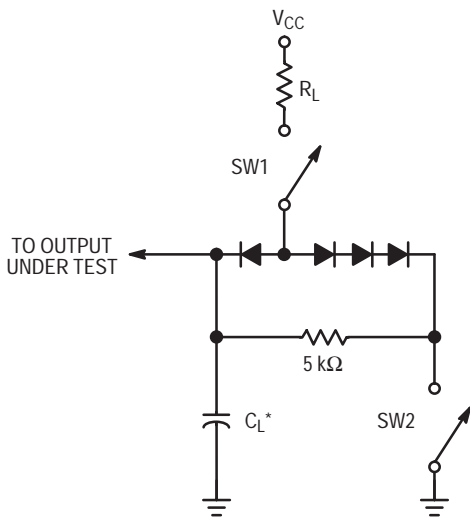


Figure 4.

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 5.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed