

SN74LS377

Octal D Flip-Flop with Enable

The SN74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

- 8-Bit High Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

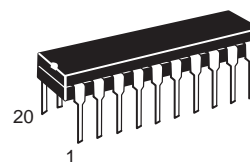
GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High			–0.4	mA
I _{OL}	Output Current – Low			8.0	mA

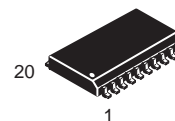


ON Semiconductor
Formerly a Division of Motorola
<http://onsemi.com>

**LOW
POWER
SCHOTTKY**



**PLASTIC
N SUFFIX
CASE 738**



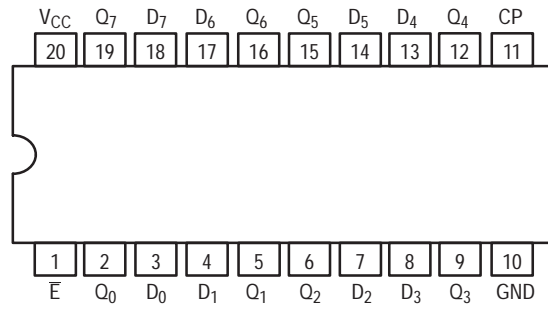
**SOIC
DW SUFFIX
CASE 751D**

ORDERING INFORMATION

Device	Package	Shipping
SN74LS377N	16 Pin DIP	1440 Units/Box
SN74LS377DW	16 Pin	2500/Tape & Reel

SN74LS377

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In-Line Package.

PIN NAMES

\bar{E}	Enable (Active LOW) Input
$D_0 - D_3$	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
$Q_0 - Q_3$	True Outputs
$\bar{Q}_0 - \bar{Q}_3$	Complemented Outputs

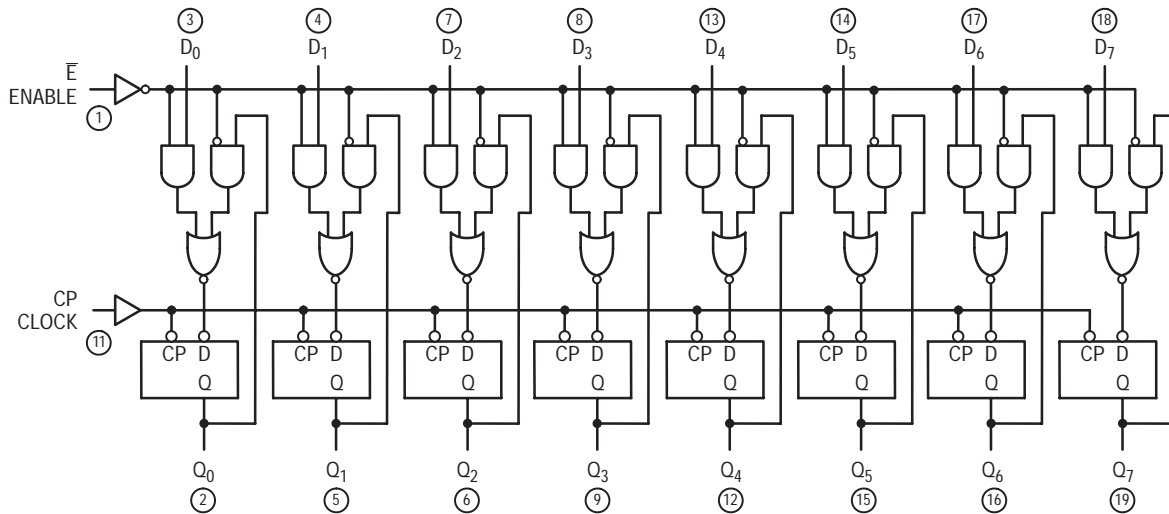
LOADING (Note a)

	HIGH	LOW
\bar{E}	0.5 U.L.	0.25 U.L.
$D_0 - D_3$	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	10 U.L.	5 U.L.
$\bar{Q}_0 - \bar{Q}_3$	10 U.L.	5 U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

LOGIC DIAGRAM



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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.7	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
			0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current			28	mA	V _{CC} = MAX, NOTE 1

NOTE: With all inputs open and GND applied to all data and enable inputs, I_{CC} is measured after a momentary GND, then 4.5 V is applied to clock.
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	40		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output		17 18	27 27	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _W	Any Pulse Width		20			ns	V _{CC} = 5.0 V
t _s	Data Setup Time		20			ns	
t _s	Enable Setup Time	Inactive — State	10			ns	
		Active — State	25			ns	
t _h	Any Hold Time		5.0			ns	

DEFINITION OF TERMS




SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the

logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

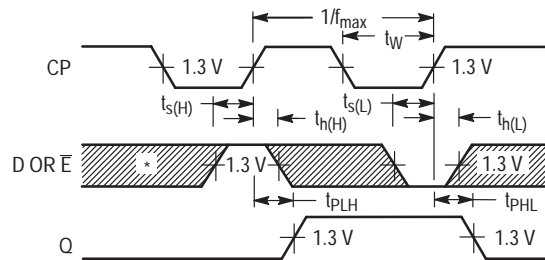
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TRUTH TABLE

\bar{E}	CP	D_n	Q_n	\bar{Q}_n
H		X	No Change	No Change
L		H	H	L
L		L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

AC WAVEFORM



*The shaded areas indicate when the input is permitted to change for predictable output performance.